Modeling and trade-off analysis of a capacitive silicon Mach-Zehnder modulator for telecom applications

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***Abstract*—This paper presents a capacitive modulator design and modeling using poly-si and silicon technologies. We propose a methodology involving the entire modulator design process, from the optical design, charge distribution calculation and small-signal RF analysis. Thus, in the case of silicon photonics modulators, the paper proposes means to optimize the trade-offs among several figures of merit. It is shown that high bandwidth operation (>30 GHz) can be achieved by sacrificing a little the modulation efficiency.**

***Index Terms*—silicon photonics, mach-zehnder, capacitive modulator, modal analysis, optical devices**

I. Introduction

Optical technologies are playing a crucial role in sustaining high bandwidth demand. Due to the exponential increase in data consumption by fixed and mobile broadband subscribers, growing bandwidth demand by high-definition video services, silicon photonics devices emerges as a potential solution for future generations of optical fiber systems, from short-reach interconnect, access and metropolitan networks [1]. One of the main advantages of silicon photonics technologies is its compatibility with complementary metal-oxide-semiconductor (CMOS) processes, which enables monolithic integration with electronic circuits. In addition, the CMOS technology has the potential for delivering reliable devices and large manufacturing scale, resulting in a low cost per device.

High-speed modulators based on the carrier depletion mechanism have been investigated for years [2]. These types of devices have modulation efficiency in the order of 2 V.cm, which requires long modulators (>3 mm) to have low V_π. Because of that, the modulator behaves as travelling-wave since its length is longer than the RF wavelength. On the other hand, capacitive modulators that use carrier accumulation mechanism can have modulation efficiency an order of magnitude higher than depletion modulators [3], decreasing the modulator length required. In this way, the modulator behaves as a lumped element which simplify its design [4].

Capacitive modulators can be implemented by using an layer of poly-Si above the silicon waveguide, with a thin oxide layer as a gate. The use of poly-Si is compatible with CMOS process and present in most silicon-on-insulator (SOI) platforms [5]. High performance capacitive modulators in this configuration have been reported in [3], [6], [7]. Due to their high bandwidth performance and modulation efficiency, such devices continue to be studied to provide increasingly efficient parameters.

The main objective of this work is to propose a design methodology to study the behaviour of the capacitive modulators with poly-Si configuration. Some device parameters such as waveguide width, doping conditions and gate thickness are studied to explore the trade-off between modulation efficiency, optical loss and modulation bandwidth.

The paper is organized in five parts. Section II addresses the device structure that will be modeled based on commercially available technologies. By means of modal analysis, in section III the waveguide width is discussed. Section IV targets the best charge distribution to assess loss and modulation efficiency. Section V performs a dynamic analysis of the modulator, from modulation efficiency to bandwidth by means of RF analysis. Finally, section VI presents a brief conclusion.

II. Device structure

Figure 1 shows the modulator schematic, where W is the waveguide width, t_{gate} is the oxide gate thickness, t_{poly} is the poly-Si thickness, t_{Si} is the silicon thickness and, finally, t_{slab} is the Si slab thickness.

It is possible to observe that the poly-Si has n-type doping and the silicon has p-type doping. The doping level becomes higher when the colors (blue and red) become darker. There-

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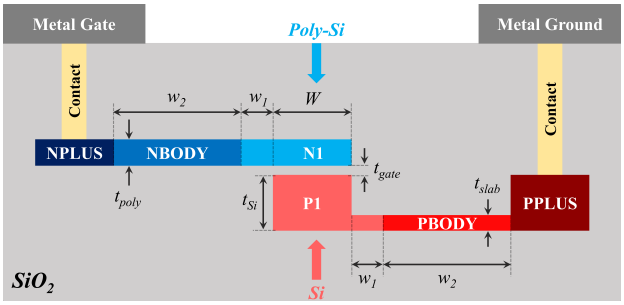


Fig. 1: Cross section view of the capacitive modulator proposed.

fore, the modulator is designated with three concentration levels.

Due to the unavailability of real poly-Si parameters for an accurate simulation, we chose to use silicon parameters in both parts of the waveguide, the top and bottom region. The device's dimensional parameters were defined as: t_{poly} = 160 nm, t_{Si} = 220 nm, t_{slab} = 70 nm and t_{gate} = 15 nm, which are in accordance with most SOI platforms. A study of the w_1 and w_2 widths will be discussed to optimize the trade-off between optical insertion loss and modulation bandwidth (access resistance). The ratio between these parameters was set to $w_1 + w_2$ = 1 μm to minimize propagation loss [7].

High PBODY/NBODY doping was set according to foundry parameters. The corresponding resistivity for each doping concentration was calculated as:

$$R = R_s \times W_i \tag{1}$$

where W_i is the width that corresponds a certain part of the device. In this case, W_i can assume the following values: W, w_1 or w_2 (see Fig. 1). The sheet resistance is obtained from experimental results in the PDK library [5].

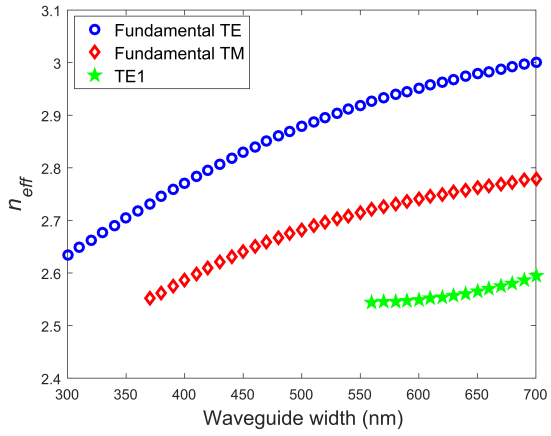
In the electrical charge simulation, reverse bias voltages from 0 to -3 volts were applied on the metal gate, while the other metal was designated as ground, as shown in Fig. 1.

Finally, all optical and charge simulations (optical and static designs) were performed using commercial LUMERICAL products. The RF simulation part (RF design) was implemented in commercial MATLAB software.

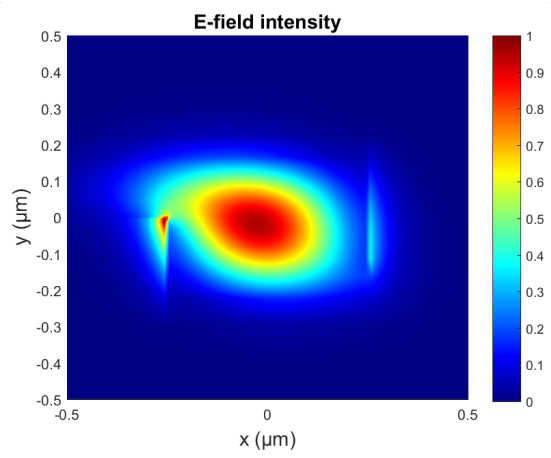
III. Optical Design

To design the device, the waveguide width (W) was swept from 300 to 700 nm in steps of 10 nm. Thus, by sweeping W, it is possible to observe the fundamental propagation mode and select a W value which provides a single propagation mode through the waveguide with high optical confinement. Figure 2 shows this analysis.

Figure 2a shows that, during the W sweep, three modes are found in the structure. The fundamental propagation TE mode is highlighted in blue. Since we want to avoid higher order modes, we choose W = 500 nm so that only the fundamental mode propagates. Values above 500 nm can provide other unwanted modes. On the other hand, values below 500 nm can



(a)



(b)

Fig. 2: (a) Effective index (n_{eff}) when the waveguide width (W) is swept from 300 to 700 nm. (b) Optical profile when W is equal to 500 nm.

result in low optical confinement and hence lower modulation efficiency. Figure 2b shows the E-field intensity profile in the waveguide. Therefore, from this point, W will be set to 500 nm.

IV. Static Modeling

After the optical design, the next step is to calculate modulation efficiency and optical loss as function of the applied voltage.

First, the charge distribution was calculated for several applied voltages using a numerical software. Doping profiles were considered homogeneous in the waveguide. Then, the charge distribution was transferred to the modal solver. The refractive index and absorption variation as function of the charge concentration is calculated using Soref's equations for 1.55 μm wavelength [8].

$$\Delta n(x,y) = -[8.8\times10^{-22} N_e(x,y) + 8.5\times10^{-18} N_h^{0.8}(x,y)] \tag{2}$$

$$\Delta\alpha(x,y) = 8.5\times10^{-18} N_e(x,y) + 6\times10^{-18} N_h(x,y) \tag{3}$$

where N_e is the electron and N_h is the hole concentration.

The effective index is found using the overlap integral [4]:

$$n_{eff} = \frac{\iint_{\infty} n(x,y)|E(x,y)|^2 ds}{\iint_{\infty} |E(x,y)|^2 ds} \quad (4)$$

where $n(x,y) = n_{Si} + \Delta n(x,y)$ and $E(x,y)$ is the fundamental mode electric field distribution. The optical insertion loss is found in the same way.

When addressing silicon modulators, the modulation efficiency ($V_\pi \times L$) is the most discussed figure of merit to evaluate the device performance. In the case of silicon photonics modulators, when subjected to a voltage, the product $V_\pi \times L$ varies non-linearly due to nonlinear variation of the silicon refractive index. In this way, the product can be calculated as [9]:

$$V_\pi \times L = \frac{\lambda}{2} \frac{dV}{dn_{eff}}\Big|_{V=V_{bias}} \quad (5)$$

where λ is the wavelength and dn_{eff} is the refractive index variation caused by the voltage variation (dV) applied on the metal gate.

A. Doping concentration analysis

In this analysis the modulation efficiency and loss were observed as function of the doping concentration. For the fundamental mode, Fig. 3 outlines the optical loss level and the modulation efficiency in relation to the carrier concentration in the waveguide, for three typical reverse bias voltage. The legend indicates the different V_{bias} for both $V_\pi \times L$ and its corresponding optical loss.

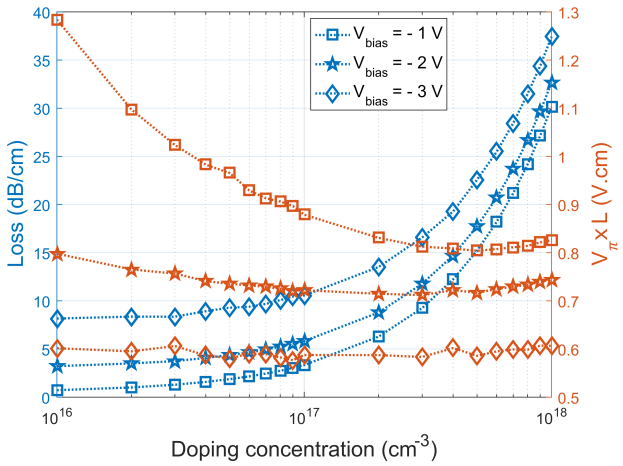


Fig. 3: Optical loss and modulation efficiency as function of the carrier concentration in the waveguide, for three V_{bias} points.

In Fig. 3, it can be observed the trade-off between optical loss and modulation efficiency. As optical modulators must be designed to operate with low optical loss and high modulating efficiency (low $V_\pi \times L$), a figure of merit (FOM, given in V.dB) is defined according to [10] to maximizes such trade-off, with the lowest value being the ideal result for this performance, as shown in Fig. 4.

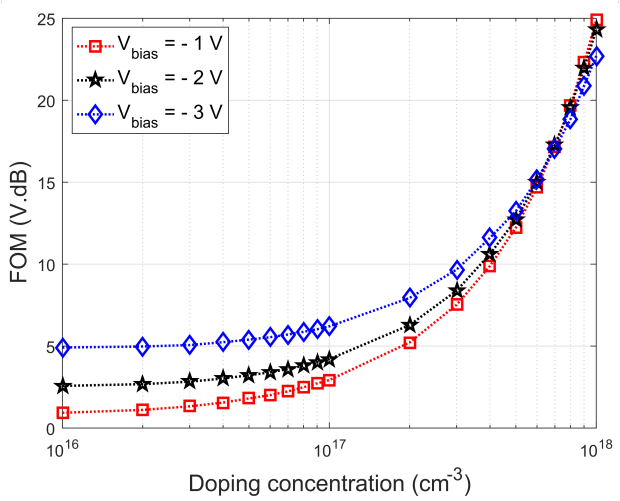


Fig. 4: FOM as function of the carrier concentration in the waveguide, for three V_{bias} points.

Observing Fig. 4, it can be seen that the lowest FOM value is in the lowest doping. However, comparing Fig. 3 and Fig. 4, it is evident that low doping is not the best choice, since low doping results in high values of $V_\pi \times L$, especially when V_{bias} = -1 V (see Fig. 3). In addition, low doping increase the access resistance, which penalize modulation bandwidth. For this reason, three candidate doping profiles for the modulator design were considered, 5×10^{16}, 1×10^{17} and 5×10^{17} cm^{-3}.

B. Doping width analysis

In the following, figures of merit were evaluated in relation to the doping width applied in the waveguide, being w_1 and w_2, as outlined in Fig. 1.

Concerning these two parameters, there is a trade-off between optical loss and modulation bandwidth. If the xBODY doping is too close to the waveguide, the optical mode will suffer higher optical loss. However, the access resistance will be lower, which improves modulation bandwidth. Figure 5 presents the estimated optical loss as function of w_2.

In Fig. 5, the loss remains constant when the w_2 value increases to a certain limit. However, from this limit, this figure of merit increases exponentially, which is not interesting for our application. The conclusion is that w_2 = 600 nm (w_1 = 400 nm) to optimize this trade-off. The same values can be found to the two other doping concentration values.

V. Dynamic Modeling

After discussing the capacitive modulator structure as well as some of its main figures of merit, this section presents a general small-signal RF analysis to estimate its modulation bandwidth.

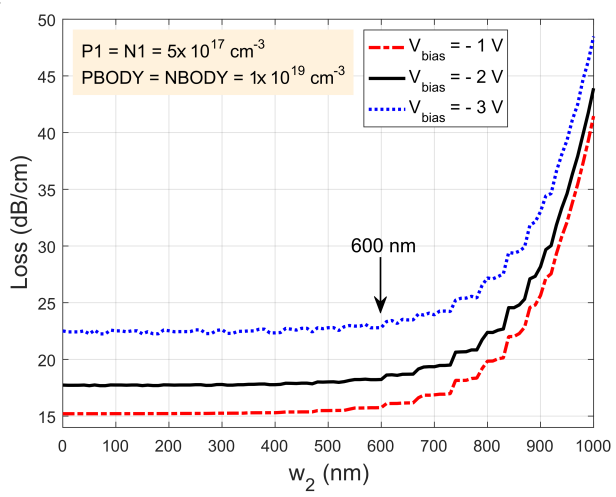


Fig. 5: Optical loss as function of w_2 for three bias voltage points.

A. Capacitance analysis

The oxide gate capacitance is obtained directly from the numerical charge solver. As an example, Fig. 6 presents the capacitance per unit length for several bias voltages.

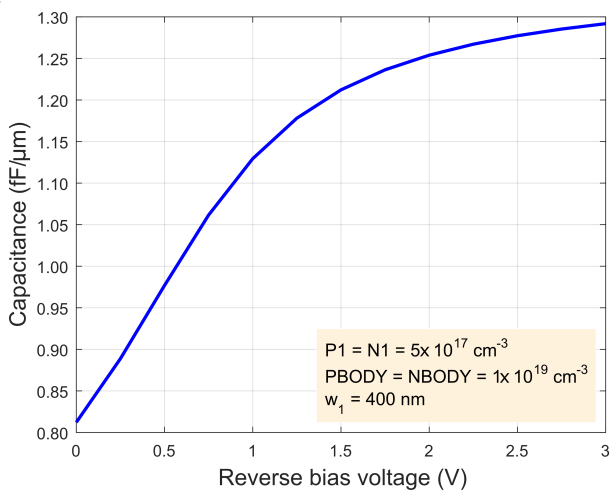


Fig. 6: Capacitance per unit length as function of V_{bias}.

In Fig. 6, when increasing the reverse bias from 0 to 3 Volts, the capacitance per unit length varies between 0.81 and 1.30 fF/μm. As modulators are designed to operate at the highest modulation speed, low capacitances are required. TABLE I summarizes the three figures of merit optimized for the three dopant concentrations analyzed.

B. Electro-optical bandwidth analysis

The EO bandwidth is calculated from the method described in [4] using the RF transmission coefficient (accounting the impedance mismatch) and the system transfer function. Figure 7 shows the RLC equivalent circuit model for the configuration proposed in this paper, where $R_{eq} = \sum_{i=1}^{4} R_i$ is the equivalent resistance resulting from the doping in different parts of the modulator.

TABLE I: Optimized parameters in different P1/N1 doping.

P1 & N1 [cm^{-3}]	$V_\pi \times L$ [V.cm]	$Loss$ [dB/cm]	C [fF/μm]
5×10^{16}	0.97 @ -1 V 0.74 @ -2 V 0.58 @ -3 V	1.87 @ -1 V 4.38 @ -2 V 9.29 @ -3 V	0.96 @ -1 V 1.23 @ -2 V 1.28 @ -3 V
1×10^{17}	0.88 @ -1 V 0.72 @ -2 V 0.58 @ -3 V	3.33 @ -1 V 5.82 @ -2 V 10.56 @ -3 V	1.0 @ -1 V 1.24 @ -2 V 1.29 @ -3 V
5×10^{17}	0.80 @ -1 V 0.71 @ -2 V 0.58 @ -3 V	15.21 @ -1 V 17.74 @ -2 V 22.58 @ -3 V	1.13 @ -1 V 1.25 @ -2 V 1.30 @ -3 V

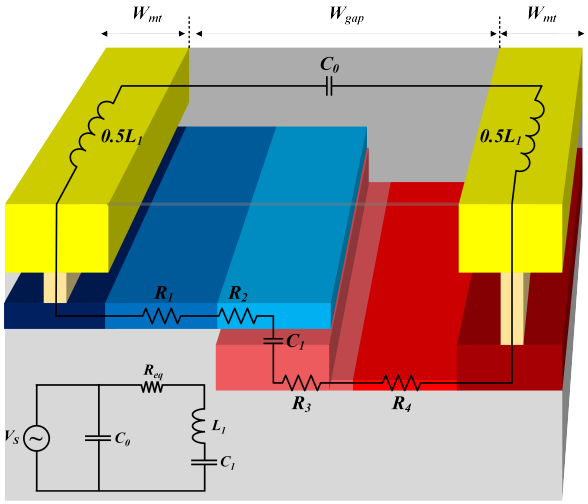


Fig. 7: Equivalent circuit model.

In Fig. 7, L_1 is the transmission line inductance, C_0 is the pad parasitic capacitance and C_1 is the capacitance on the oxide gate. In addition, it is possible to observe the configuration parameters of the transmission line, where W_{mt} is the metal width and W_{gap} is the gap between the two metal lines. Due to line and input impedance, the RF voltage transmission can be written as:

$$\Gamma(j\omega) = \frac{2Z_l}{Z_l + Z_0} \tag{6}$$

where Z_l represents the equivalent load ($R_{eq}L_1C_1||C_0$), Z_0 is the input characteristic impedance and ω is the angular frequency of the electric signal.

In addition, in (7), it is possible to observe the system transfer function $H(j\omega)$, ratio between the voltage on oxide gate and the input voltage (V_s).

$$H(j\omega) = \frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1} + j\omega L_1 + R_{eq}} \tag{7}$$

Finally, the electro-optical response can be written as:

$$S_{21_{[dB]}} = 20\log_{10}|\Gamma(j\omega)H(j\omega)| \tag{8}$$

Considering the device manufacture in the near future, the equivalent resistance as well as the waveguide doping concentration were calculated according to the parameters provided by IMEC's multi-project wafer (MPW) [5]. In this way, R_{eq} is $\sim$7.1 Ω.mm and P1/N1 is $\sim 5 \times 10^{17}$ cm^{-3}. The inductance (L_1) as a function of the operation frequency in the transmission line were calculated according to the coplanar waveguide (CPW) model proposed by Heinrich [11]. Finally, in order to provide higher bandwidth, the input characteristic impedance was set to 5 Ω, as proposed in [12].

TABLE II summarizes the figures of merit including EO bandwidth for two length cases for several t_{gate} thicknesses. For each line, W_{mt} and W_{gap} are optimized to provide the highest bandwidth.

TABLE II: Optimized parameters in different design scenarios for V_{bias} = -1 V.

t_{gate}	$V_\pi \times L$	$Loss$	EO BW (L = 0.5 mm)	EO BW (L = 1 mm)
[nm]	[V.cm]	[dB/cm]	[GHz]	[GHz]
5	0.45	16.57	9.58	7.36
15	0.80	15.21	19.35	12.45
25	1.25	14.81	25.23	15.20
35	1.64	14.66	29.35	17.19
45	2.32	14.58	32.54	18.76

In TABLE II, it is possible to note that the electro-optical bandwidth increases with the gate thickness. However, the device configuration will be the designer's choice, since the modulation efficiency behaves inversely to EO bandwidth. Figure 8 outlines the electro-optical response for three t_{gate} points. For the analysis of these three curves, the transmission line parameters W_{mt} and W_{gap} were set to $\sim$64 μm and $\sim$24 μm, respectively.

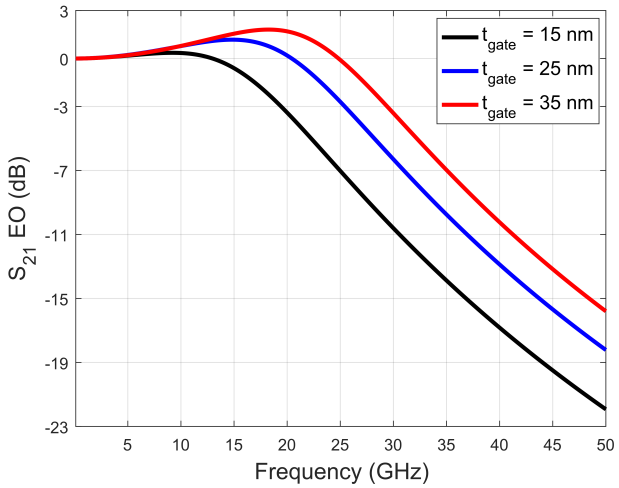


Fig. 8: Electro-optical response for V_{bias} = -1 V.

VI. Conclusion

In this paper we present a methodology to design and optimize silicon photonics modulators based on capacitive junction. Trade-offs between modulation efficiency, optical loss, modulation speed and EO bandwidth are analyzed with respect to a few modulator physical and geometrical parameters. For this, three concentration profiles (5×10^{16}, 1×10^{17} and 5×10^{17} cm^{-3}) were analyzed to better explore these trade-offs. The distance from the medium-doped regions to the waveguide was swept to optimize trade-off between access resistance (to improve modulation speed) and optical loss. The final part of the paper shows that the oxide gate thickness is crucial for improving the electro-optical bandwidth. Thus, the greater the oxide gate thickness, the lower the capacitance on the SiO_2 gate and, as a result, the greater the bandwidth offered. On the other hand, this scenario decreases the modulation efficiency and may require high voltages to drive the device. In spite of the fact that the design results have not achieved a high modulation efficiency with high modulation speed, the methodology presented here can be implemented in several silicon photonics modulators, and can be used to explore alternatives to improve these results. In addition, to improve the model accuracy, the poly-Si experimental parameters must be obtained.

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